



CORPORATE FACT SHEET

Company Overview

Jasper Design Automation is a privately-held Electronic Design Automation (EDA) company leveraging formal technologies to deliver high value/high ROI solutions for the design and verification of electronic systems and semiconductors. The company's production-proven formal verification solutions have been used on over 100 successful chip projects. System architects, logic designers, verification engineers and silicon bring-up teams are able to successfully prove protocols and executable specs; to design, explore and debug RTL; to ensure correctness of block-level functionality; and for rapid silicon validation and debug. Jasper's newly announced design solution drives greater RTL design quality and designer productivity. It is the first EDA solution for behavior-based RTL analysis and verification by logic designers that also accelerates knowledge transfer, improves design maintenance, and enables efficient reuse. Jasper solutions provide high value to both novice and advanced users.

Jasper's JasperGold® Express provides an easy-to-use, easy-to-adopt solution for migrating simulation assertions to formal verification, with the majority of implementation assertions being proven completely with push-button simplicity. Working alongside simulation, JasperGold Express ramps code quality and coverage attainment faster than simulation alone. With the fastest formal engines and powerful advanced static debugging, JasperGold® Express provides the best property specification environment available today.

Jasper's JasperGold® Verification System delivers the industry's highest proof capacity, for seamless scalability from formal assertion-based verification (ABV) to exhaustive end-to-end proofs of micro-architecture-level properties. With its automated Formal Scoreboard™ and Proof Accelerators™, JasperGold can validate complex designs that include packet-based data transportation, FIFOs, memories, caches and multiple clock domains. JasperGold delivers superior formal verification performance enabled by powerful, patented advanced formal techniques and state-of-the-art core engines. JasperGold's context-sensitive proof visibility and interactive Design Tunneling™ empower users to prove the correctness of critical design functionality.

Jasper's ActiveDesign™ is powered by formal analysis and Jasper's new Behavioral Indexing™ technology. This new solution delivers dramatic breakthroughs in design comprehension, driving higher RTL design quality and greater designer productivity. Jasper's Behavioral Indexing technology enables ActiveDesign to iteratively extract, index and store relevant design behaviors, along with the RTL, in a dynamic, executable database referred to as the Activated Design™. Activated Designs are optimized for complex yet flexible behavior-based analysis and automatic regressions, and work seamlessly with Jasper's formal property verification system, JasperGold®.

Aimed primarily at logic designers, ActiveDesign is used to confirm and index intended functional behaviors as the RTL is composed, and to easily validate complex, sometimes unintended, interactions among behaviors. This use mode is sometimes referred to as a "Designer Self Test." The powerful comprehension features in ActiveDesign help designers and verification engineers that 'inherit' a design to become intimately familiar with relevant design functionality, without any access to the original design author. Activated Designs empower any user over the life of the design, or its derivatives, to comprehend, safely modify, and retarget the RTL design for new uses.

Funding

Jasper has secured over \$27 million in four rounds of funding, from investors including Accel Partners, Cambrian Ventures, Foundation Capital, InnKap, Northzone Ventures, and ZenShin Capital. In 2004, Jasper acquired SafeLogic, a Swedish formal verification software company.

Corporate Headquarters

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Management Team

Kathryn Kranen, President and CEO

Kathryn Kranen is responsible for leading Jasper's team in successfully bringing the company's pioneering technology to the mainstream design verification market. She has 20 years EDA industry experience and a proven management track record. While serving as president and CEO of Verisity Design, Inc., US headquarters of Verisity Ltd., Kathryn and the team she built created an entirely new market in design verification. (Verisity later became a public company, and was the top-performing IPO of 2001.) Prior to Verisity, Kathryn was vice president of North American sales at Quickturn Systems. She started her career as a design engineer at Rockwell International, and later joined Daisy Systems, an early EDA company. Kathryn graduated Summa cum Laude from Texas A&M University with a B.S. in Electrical Engineering. Kathryn is serving her fifth term on the EDA Consortium board of directors, and was elected its vice chairperson. In 2005, Kathryn was recipient of the prestigious Marie R. Pistilli Women in Electronic Design Automation (EDA) Achievement Award.

Rajeev Ranjan, PhD, Chief Technology Officer

Rajeev Ranjan is responsible for developing Jasper's overall technology vision and driving the business value of formal. Prior to joining Jasper, Rajeev was CTO and VP of Engineering at Real Intent, where he led the development of their products and set the company's technical direction. Before joining Real Intent, he was in the Advanced Technology Group at Synopsys, where he co-developed the prototype for Magellan, Synopsys's formal-assisted simulation product. Rajeev has been active in the area of formal verification for over 17 years. He has served in the organization and program committee of many international conferences including DAC, ICCAD, FMCAD, and CHARME. He has published numerous articles and holds 5 patents in the area of functional verification. Rajeev received his Bachelors degree from Indian Institute of Technology, Kanpur, his Masters degree from University of Illinois at Urbana-Champaign, and his doctorate degree in formal verification from University of California at Berkeley.

Claudionor Coelho, PhD/MBA, Vice President of Engineering

Claudionor Coelho is focused on bringing strong and innovative formal verification technology to Jasper's products and to ensuring the high-quality of Jasper's tools. Claudionor has several years of experience in EDA tool development. Before joining Jasper Design-Automation, Claudionor has worked in several companies in the US, both in technical and in upper management positions, including Integrated Information Technology (NASDAQ: EGHT), performing the formal verification of a pipelined high-performance processor, and in Verplex Systems (NASDAQ: CDNS), where he directed the BlackTieTM team and was responsible for the development of OVL. He was also a founder of several successful startups, and he was a counselor for FirCapital Partners in startup strategy and technology. Claudionor obtained his BSEE (summa cum laude) and MSCS from the Federal University of Minas Gerais in Belo Horizonte, Brazil, his PhD-EE/CS from Stanford University, and his MBA from IBMEC/MG. Dr. Coelho has written award-winning papers and books, and was a contributing author to Advanced Formal Verification from Kluwer Academic Publishers. He was an Associate Professor at the Computer Science Department at the Federal University of Minas Gerais, Brazil.

Ziyad Hanna, Chief Architect and Vice President of Research

Ziyad Hanna is responsible for advancing the company's breakthroughs in formal verification technology, core engines and system architecture. Prior to joining Jasper, Ziyad was Intel senior principal engineer and the main leader of the Formal Technology Research and Development Group in the Design and Technology Solutions division at Intel Haifa. While at Intel, Ziyad was instrumental in the development of several generations of formal verification systems used on almost all Intel microprocessor designs since early 1990s. A senior IEEE member, Ziyad has been active in the area of formal verification for over 17 years, and has mentored many research projects with academia and served in various international conferences including SAT, ICCAD, DAC and ICCD. He has published more than 25 articles the formal area and holds 8 patents. He received both his B.Sc. and M.S. degrees in computer science at Tel-Aviv University, and is working towards his Ph.D. with research in "Abstract Modeling and Formal Verification of Microprocessors" at the Computing Laboratory of Oxford University.

Holly Stump, Vice President of Marketing

Holly Stump, with more than 20 years in EDA and high technology, is focused on delivering competitive business advantages to customers, leveraging Jasper's formal technology across a spectrum of applications. Her experience runs the gamut of high tech B2B marketing, business development, channel management, and international sales experience in the EDA, semiconductor and electronics industries. Prior to joining Jasper, Holly was vice president of marketing at Envis, and previously at Sequence Design. Stump cofounded or was on the executive staff of several successful EDA startups which have been acquired by industry leaders, including Logic Modeling Systems (now Synopsys), Precedence (now Mentor Graphics), and Interconnectix (Mentor Graphics). She has also held senior marketing and business development positions at Cadence Design Systems, IKOS, and Valid Logic Systems. Stump began her career designing ICs at HP, and earned her BSEE at Illinois Institute of Technology (cum laude), and MS Engineering Management at Stanford University.