



## CORPORATE FACT SHEET

### Company Overview

Jasper Design Automation is a privately-held Electronic Design Automation (EDA) company with a mission of making full formal IC verification a competitive advantage for its customers. The company's flagship product, JasperGold® Verification System, is the first verification product to deliver complete systematic verification, and accomplishes this task within predictable, finite schedule constraints. JasperGold formally verifies that complex IC design blocks meet high-level requirements defined in their specifications, and also pre-verifies IP blocks for use under all usage modes, without any testbench development.

JasperGold automatically isolates bugs with a fast, unique debugging capability. By isolating bugs earlier than simulation or formal-assisted simulation tools, and then proving the absence of bugs, JasperGold trims crucial months off design schedules. For further details on how to ensure guaranteed correctness where it matter most, and improve verification productivity, predictability and verification reuse

### **The Problem: Not all features of a design are created equal**

Traditional coverage metrics treat all parts of a design equally. There is no understanding of the importance of one feature over another. Simulation-based chip verification, by its very nature, can neither comprehend which features matter most nor guarantee 100% certainty of functional correctness. Despite the advances in testbench automation and coverage tools, simulation is still a slow, unpredictable and incomplete process. With post-tapeout chip re-design costing \$1 million or more, and delays consuming three to six additional months, design teams can never do enough traditional simulation-based verification to ensure first time functional success. Many important new product features are often dropped before tapeout due to inadequate verification. However, if companies could be certain of their verification results, the impact could be dramatic. Late stage specification changes could be made with confidence, bold new architectures could be implemented, innovation could be much more aggressive and companies could potentially leapfrog their competition. What is needed is a new tool and methodology to assure correctness where it matters most!

### **The Solution: JasperGold® - for correctness where it matters most!**

JasperGold Verification System 4.1, a block-level verification solution for RTL designs, uses state-of-the-art formal verification technology to exhaustively verify functional behaviors of RTL blocks statically, without simulation or test vectors. Jasper's Systematic Formal Verification helps design and verification teams find and remove bugs faster and easier, and ensure absolute correctness where it matters most. Working from a structured plan, users prioritize the most critical features and use formal to systematically prove them correct. Companies can then use general purpose verification methods to handle the rest of the design.

JasperGold analyzes a block against assertions and high-level requirements, and either isolates bugs that cause the requirements to fail, or proves the requirements true for all legal input sequences. It identifies many more types of bugs than traditional formal verification tools by verifying at a black-box perspective of design behavior. Only JasperGold can deliver 100% actual coverage on a complete set of functional device requirements, and can do it predictably within the verification schedule constraints.

High-level Requirements (HLRs) describe end-to-end behavior (from inputs to outputs) that a design must always or never exhibit. A powerful step up from implementation-specific assertions, HLRs represent design intent, and cover large portions of the design. Examples are: data can never be dropped or corrupted; and, flow control credits can never be leaked. If an HLR is proven true, no legal set of input vectors can cause the design to fail.

JasperGold is used during the process of RTL design, before blocks are checked in and long before simulation testbenches are available. It allows users to guarantee that their designs will meet fundamental high-level requirements, derived directly from the specification. Delivering correctness where it matters most, JasperGold provides users with insightful and specific feedback into how designs could possibly fail, influencing design creation and improving inherent design quality. Production proven with an established base of customers engaged in leading edge design, JasperGold finally answers the chip industry's critical need for higher design quality and dramatically shorter, predictable verification schedules.

## Funding

Jasper has secured a total of \$20.6 million in three rounds of funding from investors including Accel Partners, Cambrian Ventures, and Foundation Capital.

## Corporate Headquarters

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## Management Team

### **Kathryn Kranen, President and CEO**

Kathryn Kranen is responsible for leading Jasper's team in bringing the company's pioneering technology to the mainstream design verification market. She has 15 years EDA industry experience and a proven management track record, serving as president and CEO of Verisity Design, Inc., US headquarters of Verisity Ltd. Kathryn and the team she built created an entirely new market in design verification. Verisity later became a public company, and was the top-performing IPO of 2001. Prior to Verisity, Kathryn was vice president of North American sales at Quickturn Systems. She started her career as a design engineer at Rockwell International, and later joined Daisy Systems, an early EDA company. Kathryn graduated Summa cum Laude from Texas A&M University with a B.S. in Electrical Engineering. Kathryn currently serves on the EDA Consortium board of directors.

### **Craig Cochran, Vice President of Marketing**

Craig Cochran is responsible for defining and managing Jasper's worldwide marketing efforts. Prior to joining Jasper, Mr. Cochran was the Director of Marketing for Synopsys' Galaxy Design Platform, an integrated design implementation platform enabling advanced IC design. Before this, he managed Synopsys' Corporate Marketing group for four years, where he directed outbound marketing and public relations throughout the company's rapid growth to the position of market leader. Mr. Cochran spent nine years in product marketing, having launched Synopsys' formal verification and FPGA synthesis products, and managed the flagship logic synthesis product line. He holds a Bachelor of Science degree with honor in electrical engineering from the Georgia Institute of Technology.

### **Claudionor Coelho, Vice President of Engineering**

Claudionor Coelho is focused on bringing strong and innovative formal verification technology to Jasper's products and to ensuring the high-quality of Jasper's tools. Claudionor has several years of experience in EDA tool development. Before joining Jasper Design-Automation, Claudionor has worked in several companies in the US, both in technical and in upper management positions, including Integrated Information Technology (NASDAQ: EGHT), performing the formal verification of a pipelined high-performance processor, and in Verplex Systems (NASDAQ: CDNS), where he directed the BlackTie™ team and was responsible for the development of OVL. He was also a founder of several successful startups, and he was a counselor for FirCapital Partners in startup strategy and technology. Claudionor obtained his BSEE (summa cum laude) and MSCS from the Federal University of Minas Gerais in Belo Horizonte, Brazil, his PhD-EE/CS from Stanford University, and his MBA from IBMEC/MG. Dr. Coelho has written award-winning papers and books, and was a contributing author to Advanced Formal Verification from Kluwer Academic Publishers. He was an Associate Professor at the Computer Science Department at the Federal University of Minas Gerais, Brazil.