



MEDIA ADVISORY – FOR IMMEDIATE RELEASE

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Jasper Design Automation's Kathryn Kranen To Deliver Keynote Address At IP08 In Grenoble On Breakthroughs In Design Reuse And IP Delivery

Innovative Behavioral Indexing Promises Tremendous IP Integration and Design Reuse Efficiencies Along With Cost and Risk Reductions On New Design Projects

Mountain View, Calif., - December 2, 2008:

WHO:

Jasper Design Automation, the leader in successful deployment of production proven formal verification solutions, today announced that president and CEO, Kathryn Kranen, will deliver the Thursday keynote address at the IP-Based Electronic Systems Conference and Exposition in Grenoble, France, on the existing challenges and needed breakthroughs for solving scalability problems around design reuse and IP delivery.

WHAT:

The Thursday keynote, entitled, "A Breakthrough in Design Reuse and Modification," will examine how the increasing complexities of modern SoCs and short time-to-market requirements have made the efficient reuse of in-house and 3rd party IP an essential cost-saving measure. Given that some degree of modification is typically required before reuse, the root problem of efficient comprehension, modification, and re-verification in design reuse and third party IP integration will be discussed, and an emerging new technology - Behavioral Indexing - will be introduced for achieving greater IP integration and design reuse efficiencies, as well as reductions in cost and risk for new design projects.

"The internet is indexed nightly by Google and others so that users of the internet can query and source any information they want," stated Kathryn Kranen. "A new technology, called behavioral indexing, will afford end-users of digital design IP, whether third party purchased or developed in-house, the ability to query and search their designs to understand subtle nuances and design implications at an optimal level of abstraction. Applications based on

behavioral indexing promise tremendous efficiencies in IP integration, design reuse, and even design itself."

WHEN:

Thursday, December 4th, 2008, 9:00am – 9:30am

WHERE:

Room 1, World Trade Center, 5 Place Robert Schuman, Grenoble, France

For details, please visit: http://www.design-reuse.com/ip08/program/keynote_jasper.html.

WHY:

It is well-understood that IP typically requires some degree of modification for reuse, with needed modifications ranging widely: from simple mode/configuration changes, to design retargeting for a new environment, or to minor functional changes to upgrade to a new protocol or interface, and even to a major re-architecting of the design. The effective and error-free reuse of a legacy IP block/design (with or without modification) within a new ASIC or SoC requires efficient comprehension of the IP by its consumer. Unfortunately, the re-verification effort needed after the IP is modified often results in a bottleneck to the overall reuse process. Anyone interested in resolving these industry-wide concerns, and reducing complex ASIC/SOC cost and risk, will benefit from attending this keynote through greater understanding of the existing and emerging challenges, and an examination of what Behavioral Indexing can do to address and resolve them.

About Jasper Design Automation

Jasper Design Automation's production proven formal verification solutions are used by logic designers, verification engineers and silicon bring-up teams to design, explore and debug RTL, to ensure correctness of block-level functionality and for rapid silicon validation and debug. JasperGold® Verification System delivers complete "deep formal" systematic verification, ensuring correctness of critical design features without any testbench development. JasperGold Express, a "light formal" solution, complements simulation by accelerating bug-hunting and coverage attainment. For expert help with large scale formal verification deployment, RTL exploration or post-silicon debug, please visit <http://www.jasper-da.com>.

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