

Conference Coverage

EDA technologies to watch out for at DAC 2010

By Bill Murray

04/29/10

It's a bit early for DAC recommendations, but this is SCDsource's last opportunity to make some. It may occasionally feel that innovation in the EDA industry has flat-lined along with the revenue. But using our definition of innovation, it hasn't. EDA technology's objective must surely be to increase its users' effectiveness and efficiency - and continuous improvement is generally the way to get there. Innovation is a process, not an event. So, our definition encompasses not only "brand new" technology, but also significant enhancements to existing technology that make life easier for engineers. Here are our tips.

Design Task	Company	Product	Booth
High Level Synthesis	Forte	Cynthesizer	750
	Mentor	Catapult C	1383
Virtual Platforms	Wind River/Cadence	Simics/Incisive Integration	1334
Chip Synthesis	Oasys	RealTime Designer	202
Formal Verification	Jasper Design Automation	JasperGold	1337
	OneSpin Solutions	360 MV	1311
Static Timing Analysis	Magma	Tekton	602
Post-Layout Extraction	Silicon Frontline	F3D and R3D	266
Thermal/Electrical Co-Simulation	Sigrity	PowerDC Thermal	1112

Table 1: SCDsource's Innovators

High Level Synthesis

Both Forte and Mentor made our list last year, and do so again this year. Both have made significant improvements since DAC 2009. In our view, these two companies have done more than any others to bring the technology to a level of usefulness and robustness that engineers need to get a serious job done. Forte enhanced Cynthesizer's automation and control capability, and Mentor added control and SystemC capability.

[Forte boosts Cynthesizer's automation capabilities](#)

[Mentor Catapult C synthesizes control and power management](#)

Virtual Platforms

Wind River and Cadence integrated the Simics virtual platform environment with the Incisive Software Extensions (ISX), with a flow through high level synthesis to both SoC and Palladium XP. Simics is a real system simulator targeted at software engineers, who want simulation speeds in the giga-instruction per second range. And today's SoCs take more software development effort than hardware design effort. Good match.

[Cadence links Simics virtual platforms to its new Palladium XP hardware accelerator](#)

[Virtual platforms - a reality check, part 1](#)

[Virtual platforms - a reality check, part 2](#)

Chip Synthesis

Courtesy of Oasys, RealTime Designer is the biggest advance in logic synthesis in more than a

decade. According to the company, it has the capacity to handle full-chip designs of up to 100 million gates; it is 20 to 100 times faster than mainstream synthesis tools, with better area and timing QoR. How? It operates and optimizes at the chip/RTL level – not merely the block/gate optimization level. A must see.

[Chip synthesis solves the synthesis-to-P&R correlation problem](#)

Formal Verification

Jasper and OneSpin - these two on the list *again*? Why? Because their customers tell us that these are the best formal verification tools around. No further comment necessary.

[Using formal verification for SoC integration](#)

[OneSpin advances formal assertion/RTL debug automation](#)

[Mixing Formal and Dynamic Verification, Part 1](#)

[Mixing Formal and Dynamic Verification, Part 2](#)

Static Timing Analysis

Magma has caused innovative turbulence in the stagnant technology backwaters of STA. Take a look at Tekton, which boosts multi-scenario analysis performance on a single machine by upwards of 10X, without loss of accuracy. And it fits into standard flows.

[Magma's new Tekton STA tool boosts performance by upwards of 10X](#)

Post-Layout Extraction

Silicon Frontline's F3D tool delivers accuracy and speed. In one example, extraction took only 3 minutes, whereas another 'typical' 3D extractor took 7 hours to deliver the same accuracy.

[Silicon Frontline Aims at Post-Layout Verification](#)

Thermal/Electrical Co-Simulation

Sigrity's PowerDC Thermal automatic co-simulation tool eliminates the iterations inevitable in the manual simulate-and-analyze process necessitated by the traditional dual-simulator approach.

[Sigrity launches thermal/electrical co-simulation environment](#)

[Sigrity launches "beyond model extraction" package analysis tool](#)

That's all folks!

 Add Comment - please [log-in](#) to comment

SCDsource newsletter subscribers may post a comment - [Register for free!](#)

[Back to Home Page](#)