

Conference Coverage

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SCDsource's ten hot technologies to see at DAC 2009

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What's hot at DAC? SCDsource's editorial staff has selected ten technologies that we think are worth a good look. We chose them using diverse inputs – the number of hits to SCDsource's website articles, feedback from our regular engineering focus group members, and the engineering expertise of the SCDsource editorial team. A summary of the ten hot technologies is shown in figure 1, followed by more detailed descriptions of each technology or tool that made the list.

We'd like to know what you think about this list and about the companies that you visit at the DAC. Please use the comment form at the end of this article, or email us at info@scdsources.com to tell us what you found most interesting at this year's DAC. Or you can swing by the SCDsource booth (#1624, South Hall).

WHO	WHAT	SOLUTION SPACE	BOOTH/HALL
Calypto Design Systems	SLEC 4.0	System-Level Verification	1610/South
DOCEA Power	ACEplorer	System-Level Power	3143/North
Duolog Technologies	Bitwise	Intellectual Property Design and Reuse	2028/North
Forte Design Systems	Cynthesizer	High-Level Synthesis	1225/South
Jasper Design Systems	ActiveDesign	Functional Design	3767/North
Mentor Graphics	Catapult C	High-Level Synthesis	3567/North
Nusym Technology	DeNibulator	Functional Verification	622/South
OneSpin Solutions	RootCauseAnalyzer	Functional Verification	3465/North
Sigrity	XtractIM 3.0	IC Package Modeling	708/South
Silicon Frontline Technologies	F3D and R3D	Physical Design & Verification	3165/North

Figure 1 – List of ten top hot technology suppliers to see at DAC (Source: SCDsource)

Calypto SLEC 4.0

The Calypto SLEC sequential logic equivalence checker is the only tool that performs formal functional verification at the electronic system level (ESL). It compares C/C++/SystemC models with the RTL implementation code. The company recently released SLEC 4.0 with five times the capacity of its previous release, support for multiple clocks, a reduction in memory usage, and tighter integration with leading high-level synthesis (HLS) tools. SCDsource recommends that you also visit Mentor and Forte to see their HLS tools.

See Special Technology Report: [Mixing Formal and Dynamic Verification, Part 2](#)
 See First Look: [Sequential equivalence checker supports C synthesis tools](#)

DOCEA ACEplorer

The company's new XML-based ACEplorer tool automates the modeling, simulation and optimization of power characteristics at the architectural level and below. The company claims power savings of up to 90 percent versus the 10 to 20 percent achievable at RTL and physical layout. ACEplorer can model, analyze and optimize power consumption and heat dissipation; evaluate reliability risks, such as IR drop and thermal runaway; and export and manage the power intent format, UPF. The methodology guides users in modeling and refining

power models at every level throughout the flow, from the system level to silicon measurements.

See First Look article: [DOCEA tackles power early](#)

Duolog Bitwise

The company's Bitwise GUI-based product employs formalized IP metadata to automate IP-centric design reuse, using IP-XACT as a formal data interchange mechanism. This fully-automated solution captures hardware/software interfaces; validates captured data at the component and system levels; and generates multiple, consistent design views from a single data source. The tool provides a single repository for register and memory map data, accessible by the whole design team. It comes with sample generators for all common design flows including HTML, RTF (Word), FrameMaker, Structured FrameMaker, SystemVerilog, Specman 'e', ANSI C, Verilog, VHDL, and SystemC.

See Contributed Article: [Using IP standards to speed path to executable specifications](#)

Forte Design Systems Cynthesizer

Forte Design Systems' Cynthesizer is one of the two leading high level synthesis tools (Mentor Catapult C is the other one). The company recently announced enhanced control-based design support. It will show this and its other latest enhancements: support for SystemC 2.2, tools for partitioning complex hierarchical systems, automated generation of complex interfaces, memory support upgrades and scalability improvements.

See Supplier Insights: [Forte finds success with high-level synthesis](#)

Jasper ActiveDesign

ActiveDesign enables designers to confirm intended design behavior and see the consequences (both intended and unintended) of design decisions. Jasper aims to enable designers to produce higher quality RTL before it's ever checked out, so that companies no longer consume the traditional 70 percent of the development cycle to verify RTL and find bugs. The tool automatically generates waveform representations of design behavior. It employs Jasper's Behavioral Indexing technology to capture and store intended behavior in an executable database, where it can be accessed to evaluate the impact of design changes and to facilitate reuse.

See First Look: [Formal technology fuels 'behavior-based' RTL analysis](#)

Mentor Catapult C

Mentor's Catapult C is one of the two leading high level synthesis tools (Forte Cynthesizer is the other). The company recently enhanced the tool with the ability to synthesize control logic and power management functionality. The tool also has a patent-pending automated verification flow that enables easy debug of the RTL against C. The company claims that this is a significant step to full-chip synthesis. Thales Alenia Space co-piloted the specification with Mentor.

See First Look: [Mentor Catapult C synthesizes control and power management](#)

Nusym

Nusym is the only company to appear in our hot ten list for two consecutive years, because the hit rate on the SCDsource First Look merits it. Nusym is developing an "intelligent verification" approach that employs design insight to automatically drive rapid verification closure. The company is focused on moving verification coverage beyond the 70 to 80 percent coverage mark by automatic means.

See First Look: [Nusym promises high coverage with 'intelligent verification'](#)

See Conference Coverage: [Ten top technology developments to see at DAC 2008](#)

OneSpin Solutions RootCauseAnalyzer

OneSpin is showcasing its RootCauseAnalyzer tool, which automates the analysis and debug of formal SystemVerilog assertions and RTL code. The company claims that it eliminates a great deal of manual effort, and it enables the debug of complex, hierarchically-coded, specification-level assertions. It is an integral part of the company's 360 MV family, which offers five different, interoperable formal assertion-based verification solutions covering early automatic RTL analysis and fast block-level verification to highest-quality gap-free verification using SystemVerilog assertions.

See First Look: [OneSpin advances formal assertion/RTL debug automation](#)

Sigrity XtractIM 3.0

Sigrity's XtractIM 3.0 GUI-based package analysis tool claims to have the fastest, highest

capacity analysis engines, complemented by package design automation. The tool goes beyond extraction to enable clear identification of potential performance issues. The tool's new capabilities enable package designers to assess the performance of signal and power delivery nets intuitively, characterize a broader set of package types, and extract electrical models with improved accuracy. And it provides a way to immediately assess whether the package is likely to have a problem, eliminating downstream simulation and expert analysis.

See First Look: [Sigrity launches "beyond model extraction" package analysis tool](#)

Silicon Frontline


Silicon Frontline Technologies recently launched two products aimed at post-layout verification: F3D (Fast 3D) for fast 3D extraction, and R3D (Resistive 3D) for 3D extraction and analysis of large resistive structures, such as power devices. Both tools claim to be "guaranteed accurate" solutions for full-chip 3D parasitic extraction with performance equivalent to 2D tools. F3D and R3D generate a fully annotated SPICE netlist with parasitics for use by downstream tools. The company is targeting CAD, TCAD and post-layout verification engineers who might otherwise build a test chip to measure critical silicon characteristics.

See First Look: [Silicon Frontline Aims at Post-Layout Verification](#)

Notable DAC Panels and Events

Here is a list of panels, special sessions, tutorials and events that SCDsource believes is worth mentioning:

- Technical Panel: [System Prototypes: Virtual, Hardware or Hybrid?](#)
Also check out Special Technology Report: [Virtual platforms - a reality check, part 1](#) and [Virtual platforms - a reality check, part 2](#)
- Special Plenary Panel: [How Green Is My Silicon Valley](#)
- Special Session: [The Tool Shows That My Design is Wrong. But Where is the Bug?](#)
Also check out Special Technology Report: [Mixing Formal and Dynamic Verification, Part 1](#) and [Mixing Formal and Dynamic Verification, Part 2](#)
- Tutorial #1: [Low-Power SOC Design: State of the Art and Directions](#)
Also check out Special Technology Report: [Automating low-power design - a progress report](#)
- Workshop: [Workshop for Women in Design Automation \(WWINDA\): Career Crossroads - Who Has the Map?](#)
- Workshop: [Multiprocessor System-On-Chip: Current Trends and the Future](#)
- Panel: [Guess, Solder, Measure, Repeat - How Do I Get My Mixed-Signal Chip Right?](#)
- Additional Meeting: [Silicon IP - Beyond Chips to Systems. What are the Challenges and Opportunities?](#)

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