

First Look

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Formal technology fuels 'behavior-based' RTL analysis

By Richard Goering

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If verification occurred interactively as RTL code is developed, the results could include higher quality code and less overall verification effort. That's what Jasper Design Automation is promising this week (Jan. 19) with ActiveDesign, a "behavior-based" RTL analysis and verification tool aimed at logic designers with no formal verification expertise.

Working from partially coded RTL, ActiveDesign automatically generates waveform representations of design behavior. Designers can confirm intended design behavior and see the unintended consequences of design decisions. Through a process called "behavioral indexing," intended behavior is then stored in an executable database, called an Activated Design, where it can be accessed to evaluate the impact of design changes and to facilitate reuse.

ActiveDesign is a first-of-its-kind tool but is a natural complement to existing RTL design methodologies, according to Jasper. "There is no change to your RTL methodology," said Kathryn Kranen, Jasper president and CEO, "but getting immediate feedback on the consequences of how you wrote your RTL is revolutionary."

"This is about arming designers to produce higher quality RTL before it's ever checked in, so you don't spend the traditional 70 percent of the development cycle trying to verify bugs that slipped into the RTL," Kranen said. "We haven't met a designer who doesn't want to deliver higher quality RTL, but they're just crippled right now."

As of today, Kranen said, RTL design blocks need to be fairly complete before verification can begin, with pathways between primary inputs and outputs connected. And a verification infrastructure, along with a testbench, needs to be in place. ActiveDesign, in contrast, "lets you iteratively confirm the behavior that you're creating on the fly, without depending on other people to provide test environments for you," she said.

The most obvious benefit of ActiveDesign is the possibility of reducing overall verification time. Also important, said Kranen, is enhanced "design comprehension" due to the availability of waveforms and indexed behavior. Because the executable database captures design intent, designers who had no role in the original RTL development should be able to understand the intended behavior. And this, in turn, "takes away the risk of reusing a design," Kranen said.

ActiveDesign is by no means the first RTL analysis tool that uses formal techniques – there are many, ranging from static "lint" checkers to cross-domain clocking (CDC) verification tools. But existing RTL analysis tools focus on structural information, Kranen said, while ActiveDesign evaluates functionality and behavior. Moreover, in contrast to batch RTL analysis tools that spit out reports, ActiveDesign "is a very rich interactive system that enables behavior-based verification analysis," she said.

Starting with waveforms

ActiveDesign uses formal analysis techniques, along with Jasper's visualization technology, to produce waveforms from SystemVerilog, Verilog or VHDL RTL code. No testbench is required. From the waveforms, designers can evaluate whether their code creates desired behaviors. If not, they can modify the RTL code until the desired behavior is attained, and they can immediately view the impact of any design changes.

The waveforms allow designers to identify "scenarios" they feel are important. A scenario is basically a sequence of events that place the design in a given state. For example, a scenario might describe the behavior of a read path from a memory bank into cache. Designers can manipulate waveforms so they match the desired scenario.

"Just by mixing and matching behaviors, it [ActiveDesign] will produce scenarios hundreds of cycles long with a great degree of complexity," Kranen said. "This is when jaws drop. Designers say, 'wow, it would have taken days to try to create the stimulus that would get me to that point.'"

Once the designer is satisfied with the waveforms, the tool indexes the associated behavior and stores it in the executable database (Figure 1). Scenarios can become building blocks that help designers evaluate possible changes to current or future designs. For example, a designer could

see what happens if a memory access is shifted from bank 2 to bank 3. Because the database is executable, all scenarios are regenerated automatically when a design change is made.

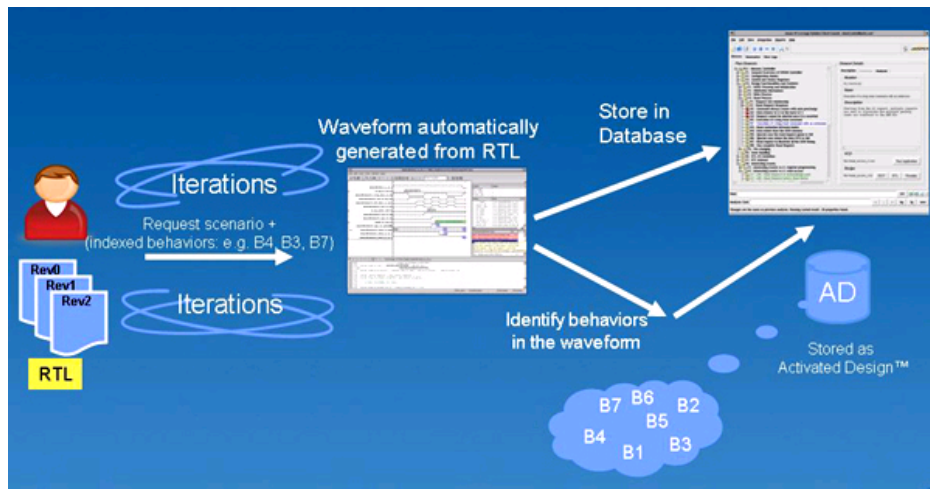


Figure 1 – ActiveDesign generates waveforms and stores behavioral information in an executable database.

ActiveDesign produces “implication analysis” reports that show the impact of design changes on indexed behaviors and scenarios. There are three classifications: “unaffected” (reproducible with the same latency), “potentially affected” (reproducible but temporally altered), and “broken” (not reproducible).

So what’s in the database? “It’s really kind of an enlarged design,” Kranen said. An Activated Design database stores the information needed to produce and combine waveforms, and can include English language comments added by the designer. It uses the XML format and outputs reports in HTML. “We really bent over backwards to use industry standard languages,” she said.

Creating properties

In effect, users are creating properties by editing and extending waveforms. Designers don’t have to know anything about properties, but if they do, they can optionally code properties directly or edit them. Jasper’s JasperGold formal verification tool can be used downstream to verify the properties. However, JasperGold is not required to run ActiveDesign.

There’s an important distinction between JasperGold and ActiveDesign. JasperGold focuses on exhaustive proofs of high-level properties. ActiveDesign is not a formal model checker, and does not provide exhaustive proofs. Thus, it doesn’t replace the need for formal model checking. Kranen said, however, that ActiveDesign can potentially reduce or replace the need for block-level simulation.

While ActiveDesign sets a new direction for Jasper, more may be in store. “Behavioral indexing opens up a whole new world of opportunity for us. You will hear more in this realm,” Kranen said.

Currently in beta sites, ActiveDesign is slated for availability in March, with prices starting at \$140,000. It will be demonstrated at the [EDS Fair](#) in Japan Jan. 22-23 and at the Design and Verification Conference ([DVCon](#)) in San Jose, Calif. Feb. 24-26.

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